type (P type for example) to form the vertical sections **32** or **36**. The second conductivity type dopant may be implanted using a thick implant mask or a focused ion beam.

In one embodiment, for a 1000 volt device with a 10 micron pitch, the epitaxial layer could have a thickness of 55 microns and a dopant concentration of 4E15/cm3 (1.2 ohm cm) on an N+ substrate. Boron is then implanted with the implant energy varied from several Kev to about 70 Mev to distribute the boron vertically in sections **32** or **36**. The total dose required is about 2E13/cm2 for a masked implant, and about half this value for a focused ion beam implant.

While preferred embodiments of the present invention have been described, it is to be understood that the embodiments described are illustrative only and the scope of the invention is to be defined solely by the appended claims when accorded a full range of equivalence, many variations and modifications naturally occurring to those of skill in the art from a perusal hereof.

What is claimed is:

1. A MOSFET having a voltage supporting region comprising a horizontal layer, said layer comprising a first semiconductor type having a plurality of discontinuous floating regions of a second semiconductor type, wherein the regions are spaced in three dimensions.

2. The MOSFET of claim **1** wherein said floating regions are uniformly positioned throughout said layer.

3. A semiconductor device having a voltage supporting region comprising a horizontal layer, said layer comprising a first semiconductor type having floating regions of a second semiconductor type wherein said regions are oblate spheroids positioned in horizontal rows and vertical columns.

4. The semiconductor device of claim **3** wherein said device is a vertically conducting high voltage MOSFET.

5. The semiconductor device of claim **3** wherein said layer has an avalanche breakdown voltage wherein substantially the entire thickness of said layer is depleted before said layer reaches said avalanche breakdown voltage.

6. The semiconductor device of claim **3** wherein said layer has an avalanche breakdown voltage, and wherein if the electric field in said layer reaches said avalanche breakdown voltage, the electric field over substantially the entire vertical thickness of said layer reaches said avalanche breakdown voltage.

7. A horizontal blocking layer for a vertically conducting MOSFET comprising a layer of first semiconductor type having a plurality of discontinuous and uniformly positioned floating regions of a second semiconductor type, wherein the regions are spaced in three dimensions.

8. The blocking layer of claim **7** wherein said floating regions are substantially spheroids or oblate spheroids and are positioned uniformly to form horizontal rows and vertical columns within said layer.

9. A MOSFET comprising:

a source and gate region;

a drain region; and

a layer between said source and gate region and said drain region and adjacent said source and gate region,

said regions and layer being horizontal and substantially parallel and extending laterally across said MOSFET,

said layer comprising a first semiconductor type having a plurality of discontinuous floating regions of second semiconductor type, wherein said floating regions are spaced in three dimensions.

10. A MOSFET comprising:

a source and gate region;

a drain region; and

a layer between said source and gate region and said drain region and adjacent said source and gate region,

said regions and layer being horizontal and substantially parallel and extending laterally across said MOSFET,

said layer comprising a first semiconductor type having floating regions of second semiconductor type,

said floating regions are substantially spheroids or oblate spheroids and are positioned uniformly to form horizontal rows and vertical columns within said layer.

11. A vertically conducting high voltage MOSFET having a voltage supporting region comprising a horizontal layer of a first semiconductor type having floating regions of a second semiconductor type, wherein said floating regions are oblate spheroids, said MOSFET having an avalanche breakdown voltage, wherein if the electric field in said layer reaches said avalanche breakdown voltage, the electric field over substantially the entire vertical thickness of said layer reaches said avalanche breakdown voltage.

12. A semiconductor device having a voltage supporting region comprising a horizontal layer of first conductivity type, and having oblate spheroids of second conductivity type dispersed in the layer for improving the breakdown voltage of the semiconductor device.

* * * * *